IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) Control circuitry for adjusting a power supply level of a digital processing component having varying operating frequencies, said control circuitry comprising:

a plurality of delay cells coupled in series, each of said plurality of delay cells having a delay based on a value of the power supply level, such that a clock edge applied to an input of one of the delay cells ripples sequentially through said plurality of delay cells; and

power supply adjustment circuitry capable of adjusting the power supply level, said power supply adjustment circuitry operable to (i) monitor outputs of at least a first delay cell and a second delay cell immediately following the first delay cell, (ii) determine that said clock edge has reached an output of said first delay cell and has not reached an output of said second delay cell [[when]] <u>in response to</u> a next sequential clock edge [[is]] <u>being</u> applied to the delay cell input, and (iii) generate a control signal capable of adjusting the power supply level based on the determination.

2. (Cancelled).

3. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 1 wherein a total delay from said delay cell input to said first delay cell output is greater than a maximum delay of said digital processing component scaled by a constant factor.

4. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 1 wherein said power supply adjustment circuitry increases the power supply level if said clock edge has not reached said first delay cell output.

5. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 1 wherein said power supply adjustment circuitry decreases the power supply level if said clock edge has reached said second delay cell output.

6. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 1 wherein said power supply adjustment circuitry is further operable to monitor outputs of at least a third delay cell immediately preceding the first delay cell, said first delay cell, said second delay cell, and a fourth delay cell immediately following the second delay cell.

7. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 6 wherein said power supply adjustment circuitry is further operable to determine that said clock edge has reached an output of said third delay cell and said first delay cell output and has not reached said second delay cell output.

8. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 7 wherein said power supply adjustment circuitry increases the power supply level in relatively large incremental steps if said clock edge has not reached said third delay cell output.

9. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 8 wherein said power supply adjustment circuitry increases the power supply level in relatively small incremental steps if said clock edge has reached said third delay cell output but has not reached said first delay cell output.

10. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 7 wherein said power supply adjustment circuitry decreases the power supply level in relatively large incremental steps if said clock edge has reached said second delay cell output and said fourth delay cell output.

11. (Previously Presented) The control circuitry for adjusting a power supply level as set forth in Claim 10 wherein said power supply adjustment circuitry decreases the power supply level in relatively small incremental steps if said clock edge has reached said second delay cell output but has not reached said fourth delay cell output.

12. (Currently Amended) A method of operating control circuitry for adjusting a power supply level of a digital processing component having varying operating frequencies, said method of operating said control circuitry comprising the steps of:

applying a clock edge to an input of one of a plurality of delay cells coupled in series, each of said plurality of delay cells having a delay based on a value of the power supply level, said applied clock edge rippling sequentially through said plurality of delay cells;

monitoring outputs of at least a first delay cell and a second delay cell immediately following the first delay cell;

determining that said clock edge has reached an output of said first delay cell and has not reached an output of said second delay cell [[when]] <u>in response to</u> a next sequential clock edge [[is]] <u>being</u> applied to the delay cell input; and

generating a control signal capable of adjusting the power supply level based on the determination.

13. (Cancelled).

14. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 12 wherein a total delay from said delay cell input to said first delay cell output is greater than a maximum delay of said digital processing component scaled by a constant factor.

15. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 12 further comprising the step of increasing the power supply level if said clock edge has not reached said first delay cell output.

16. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 12 further comprising the step of decreasing the power supply level if said clock edge has reached said second delay cell output.

17. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 12 further comprising the step of monitoring outputs of at least a third delay cell immediately preceding the first delay cell, said first delay cell, said second delay cell, and a fourth delay cell immediately following the second delay cell.

18. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 17 further comprising the step of determining that said clock edge has reached an output of said third delay cell and said first delay cell output and has not reached said second delay cell output.

19. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 18 further comprising the step of increasing the power supply level in relatively large incremental steps if said clock edge has not reached said third delay cell output.

20. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 19 further comprising the step of increasing the power supply level in relatively small incremental steps if said clock edge has reached said third delay cell output but has not reached said first delay cell output.

21. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 18 further comprising the step of decreasing the power supply level in relatively large incremental steps if said clock edge has reached said second delay cell output and said fourth delay cell output.

22. (Previously Presented) The method of operating control circuitry for adjusting a power supply level as set forth in Claim 21 further comprising the step of decreasing the power supply level in relatively small incremental steps if said clock edge has reached said second delay cell output but has not reached said fourth delay cell output.

23. (Currently Amended) A digital circuit comprising:

a digital processing component capable of operating at different clock frequencies;

an adjustable clock source capable of supplying variable clock frequencies to said digital processing component;

an adjustable power supply capable of supplying a variable power supply level to said digital processing component; and

control circuitry for adjusting the power supply level comprising:

a plurality of delay cells coupled in series, each of said plurality of delay cells having a delay based on a value of the power supply level, such that a clock edge applied to an input of one of the delay cells ripples sequentially through said plurality of delay cells; and

power supply adjustment circuitry capable of adjusting the power supply level, said power supply adjustment circuitry operable to (i) monitor outputs of at least a first delay cell and a second delay cell immediately following the first delay cell, (ii) determine that said clock edge has reached an output of said first delay cell and has not reached an output of said second delay cell [[when]] <u>in response to</u> a next sequential clock edge [[is]] <u>being</u> applied to the delay cell input, and (iii) generate a control signal capable of adjusting the power supply level based on the determination.

24. (Cancelled).

25. (Previously Presented) The digital circuit as set forth in Claim 23 wherein a total delay from said delay cell input to said first delay cell output is greater than a maximum delay of said digital processing component.

26. (Previously Presented) The digital circuit as set forth in Claim 23 wherein said power supply adjustment circuitry increases the power supply level if said clock edge has not reached said first delay cell output.

27. (Previously Presented) The digital circuit as set forth in Claim 23 wherein said power supply adjustment circuitry decreases the power supply level if said clock edge has reached said second delay cell output.

28. (Previously Presented) The digital circuit as set forth in Claim 23 wherein said power supply adjustment circuitry is further operable to monitor outputs of at least a third delay cell immediately preceding the first delay cell, said first delay cell, said second delay cell, and a fourth delay cell immediately following the second delay cell.

29. (Previously Presented) The digital circuit as set forth in Claim 28 wherein said power supply adjustment circuitry is further operable to determine that said clock edge has reached an output of said third delay cell and said first delay cell output and has not reached said second delay cell output.

30. (Previously Presented) The digital circuit as set forth in Claim 29 wherein said power supply adjustment circuitry increases the power supply level in relatively large incremental steps if said clock edge has not reached said third delay cell output.

31. (Previously Presented) The digital circuit as set forth in Claim 30 wherein said power supply adjustment circuitry increases the power supply level in relatively small incremental steps if said clock edge has reached said third delay cell output but has not reached said first delay cell output.

32. (Previously Presented) The digital circuit as set forth in Claim 29 wherein said power supply adjustment circuitry decreases the power supply level in relatively large incremental steps if said clock edge has reached said second delay cell output and said fourth delay cell output.

33. (Previously Presented) The digital circuit as set forth in Claim 32 wherein said power supply adjustment circuitry decreases the power supply level in relatively small incremental steps if said clock edge has reached said second delay cell output but has not reached said fourth delay cell output.